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Question Paper Code : 90570

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Fifth/Sixth Semester

Electronics and Communication Engineering

CEC 337 — DSP ARCHITECTURE AND PROGRAMMING

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the addressing modes that can enhance DSP implementations?

2. State the role of the program sequencer.

3. Give examples for parallel store and add/subtract instructions of the TMS320C54xx processors.

4. Mention the sizes of data memory and program memory of the TMS320C54xx processors?

5. State the purposes of *.ref* and *.bss* assembly directives.

6. List the interrupt sources in TMS320C6X.

7. What are vector files?

8. Define an adaptive filter?

9. What is voice scrambling?

10. Mention the applications of graphic equalizer.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the working principle of a MAC unit with a diagram and discuss the factors to be considered when designing a MAC unit. (7)

(ii) Discuss various operations involved in address generation. (6)

Or

(b) Discuss parallelism and pipelining-based techniques to increase the speed of operation of DSP architectures.

12. (a) (i) Describe the functionality of the central processing unit of the TMS320C54xx processors with the functional diagram. (7)

(ii) Explain the immediate, absolute, and direct addressing modes of the TMS320C54xx processors. (6)

Or

(b) (i) Explain the six-stage pipeline execution of the TMS320C54xx processors. (7)

(ii) Explain the hardware timer with the logical diagram and timer control register details. (6)

13. (a) (i) Draw and explain the functional block diagram of TMS320C6713. (7)

(ii) Describe the indirect and circular addressing modes supported by TMS320CX processors. (6)

Or

(b) Discuss the features of the TMS320C67xx DSP Starter Kit with its block diagram.

14. (a) Elaborate on the procedure to build applications, and debug and test them using the DSK board with Code Composer Studio.

Or

(b) With the block diagram explain the procedure to implement an FIR filter and implement it using TMS320C54xx.

15. (a) Design a system for DTMF signal detection using appropriate signal processing techniques and algorithms.

Or

(b) Develop a speech synthesis system using linear prediction of speech signals.

PART C — (1 × 15 = 15 marks)

16. (a) Design a real-time adaptive noise cancellation system for EEG signal enhancement.

Or

(b) Design an automatic speaker recognition system for voice-based attendance.

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